REMARKS

Claims 1, 7, 13 and 17 are amended herein. Claims 1-8 and 10-23 remain pending in the application.

Finality of the Office Action

The Office Action Summary indicates the Office Action is non-final. However, page 9 of the Office Action indicates Finality. The Applicants are unclear as to the present standing of the Application. Therefore, if the Application is under a Final rejection, Applicants respectfully request entry of this Amendment and withdrawal of the finality, because no new issued are raised, nor is further search required.

Claims 1-8, 10-13, 15, 16, 20, 21 and 23 over Persaud and Wu

In the Office Action, claims 13, 15 and 16 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud, UK Patent Application No. GB2074762 ("Persaud") in view of Wu et al., Patent No. 5,659,715 ("Wu"), with claims 1-8, 10-12, 20, 21 and 23 rejected as obvious over Wu in view of Persaud. Applicants respectfully traverse the rejection.

Claims 1-8, 10-13, 15, 16, 20, 21 and 23 recite, *inter alia*, a second agent receiving a memory access clock signal from a first agent.

Persaud appears to teach a system and method for accessing a common memory by a plurality of processors (Persaud, Abstract). A master processor can access its own memory or any of the slave memories (Persaid, Abstract). The master processor generates synchronizing signals which are applied over a backplane to each of the slave processors (Persaud, page 2, lines 45-47). Handshaking between the master and slave processors is used to control which processor obtains access to an entire particular slave's memory at any point in time (Persaud, page 2, lines 8-21). The master processor accesses memory that is dedicated to a slave processor since each processor/memory combination is contained on a common card (Persaud, page 1, lines 39-43).

The Office Action correctly acknowledged that Persaud fails to teach an external non-dedicated memory nor a first and second agent accessing

different portions of a shared memory simultaneously. However, the Office Action relies on Wu to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention. The Applicants respectfully disagree.

Wu appears to teach a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (WU, Fig. 3) Thus, the CPU, the graphics controller and the common memory are synchronized to pass data and address information therebetween with a common clock signal.

Persuad teaches slave processor clocks that are referenced to the master processor clocks for synchronization. However, all clock signals are generated locally at each processor, with the slave processors generating their own clock signals (Persuad, page 2, lines 45-47).

Neither Persuad nor Wu disclose, teach, or suggest a second agent receiving a memory access clock signal from a first agent, as claimed by claims 1-8, 10-13, 15, 16, 20, 21 and 23.

A benefit of having a second agent access a shared memory with a clock signal received from a first agent is, e.g., synchronization through simplicity. Applicants' system requires only a single memory access clock, with all agents sharing the signal. A single memory access clock signal synchronizing all agents' access to a shared memory possibly eliminates wasted clock cycles during a transfer of access from a first agent to a second agent. In contrast, Persaud requires the use of a dedicated clock generator for each agent. Having multiple clock generators creates the problem of synchronization (as discussed by Persaud, page 3, lines 1-22).

Accordingly, for at least all the above reasons, claims 1-8, 10-13, 15, 16, 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 14, 17-19 and 22 over Persaud and Wu in view of Hughes

In the Office Action, claims 14, 17-19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud and Wu in view of Hughes, U.S. Patent No. 5,6784,582 ("Hughes"). The Applicants respectfully traverse the rejection.

Claims 14-15 are dependent on claim 13 and are patentable for at least the same reasons as claim 13.

Claims 14, 15, 17-19 and 22 recite, *inter alia*, a second agent receiving a memory access clock signal from a first agent.

As discussed above, Persaud and Wu fail to teach a second agent receiving a memory access clock signal from a first agent, as claimed by claims 14 and 15.

Hughes appears to disclose an arbiter for controlling access to an entire shared synchronous memory by a processor complex, a refresh unit, an internal bus, and a core bus (See Hughes, col. 4, lines 1-29; Figure 2). The access requests to the SDRAM are based on size, location, and direction of the transfer (Hughes, col. 6, lines 39-57). Hughes' processor complex provides a memory clock signal in addition to memory access request information (See Hughes, col. 4, lines 49-58). This memory clock signal is the only clock signal provided to shared memory (See Hughes, col. 4, lines 55-58; Figure 2). Other users of the shared memory (the refresh unit, internal bus, and core bus) provide only memory access request information, i.e., starting address, size, and a direction (See Hughes, col. 5, lines 35-45). The other users of the shared memory do not provide any clock signal to shared memory (See Hughes, Figures 2 and 3).

Neither Persaud, Wu nor Hughes disclose, teach, or suggest a second agent receiving a memory access clock signal from a first agent, as claimed by claims 14, 15, 17-19 and 22.

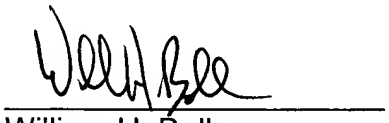
Accordingly, for at least all the above reasons, claims 14, 15, 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8, and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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